AMENDMENTS TO THE CLAIMS

1. (Currently Amended) An image processing apparatus for wafer inspection tool to perform visual inspection by die to die comparison and~~/or~~ cell to cell comparison, using serial image data of an object which has a plurality of dice each having an identical circuitry pattern formed thereon or a plurality of cells on a die each having an identical circuitry pattern formed thereon, said image processing apparatus comprising:

a plurality of processors for performing parallel processing;

means for cutting serial image data into a plurality of cutout image data, said cutout image data including a forward end overlap and a rear end overlap at cutout boundaries and having a predetermined data size;

means for distributing said cutout image data to said plurality of processors; and

means for assembling results of processing performed by said plurality of processors,

wherein said forward end overlap is the sum of an overlap margin for operation processing and the maximum cell pitch of a plurality of cell pitches in cell to cell comparison inspection, and said rear end overlap is an overlap margin for operation processing ~~greater than a pitch of the cell in cell to cell comparison inspection~~.

2. (Original) The image processing apparatus for wafer inspection tool according to claim 1, wherein said means for cutting serial image data has a function to cut out said cutout image data including said forward end overlap and said rear end overlap according to a line address of head position of cutout image data and a cutout width, wherein said line address is less by said forward end overlap than a boundary between said image data and the preceding image data and said cutout width is the sum of said cutout image data, forward end overlap and rear end overlap.

3. (Original) The image processing apparatus for wafer inspection tool according to claim 2, further comprising:

means for storing a pre-calculated line address of head position of said cutout image data and a pre-calculated cutout width of said cutout image data into a memory; and

means for comparing a line address that is now counted with said pre-calculated line address stored in said memory.

4. (Original) The image processing apparatus for wafer inspection tool according to claim 1, wherein said forward end overlap is greater than a maximum cell pitch size.

5. (Original) The image processing apparatus for wafer inspection tool according to claim 1, wherein each of said processor has a function program which is configured to perform cell to cell comparison inspection by using said cutout image data distributed to said processor.

6. (Original) The image processing apparatus for wafer inspection tool according to claim 1, wherein each of said processor has a function program which is configured to perform die to die comparison inspection by using said cutout image data distributed to said processor.

7. (Currently Amended) An image processing apparatus for wafer inspection tool to perform visual inspection by die to die comparison and cell to cell comparison, using serial image data of an object which has a plurality of dice each having an identical circuitry pattern formed thereon or a plurality of cells on a die each having an identical circuitry pattern formed thereon, said image processing apparatus comprising:

a plurality of processors for performing parallel processing;

means for cutting serial image data into a plurality of cutout image data, said cutout image data including a forward end overlap and a rear end overlap at cutout boundaries and having a predetermined data size;

means for distributing said cutout image data to said plurality of processors; and

means for assembling results of processing performed by said plurality of processors,

wherein said forward end overlap is the sum of an overlap margin for operation processing and the double of a cell pitch size in cell to cell comparison inspection, and said rear end overlap is the sum of an overlap margin for operation processing and the cell pitch size ~~The image processing apparatus for wafer inspection tool according to claim 1, wherein each of said processor has a~~

~~function program which is configured to perform cell to cell and die to die hybrid comparison inspection by using said cutout image data distributed to said processor~~.

8. (Original) The image processing apparatus for wafer inspection tool according to claim 1, wherein said forward end overlap is greater than the double of said pitch of the cell in cell to cell comparison inspection and said rear end overlap is greater than said pitch of the cell.